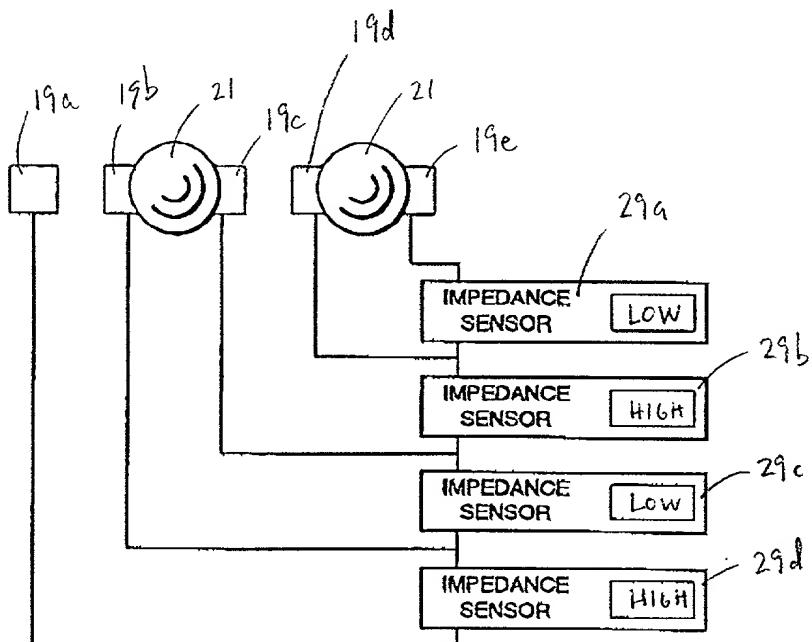


F16. 1



F16. 3

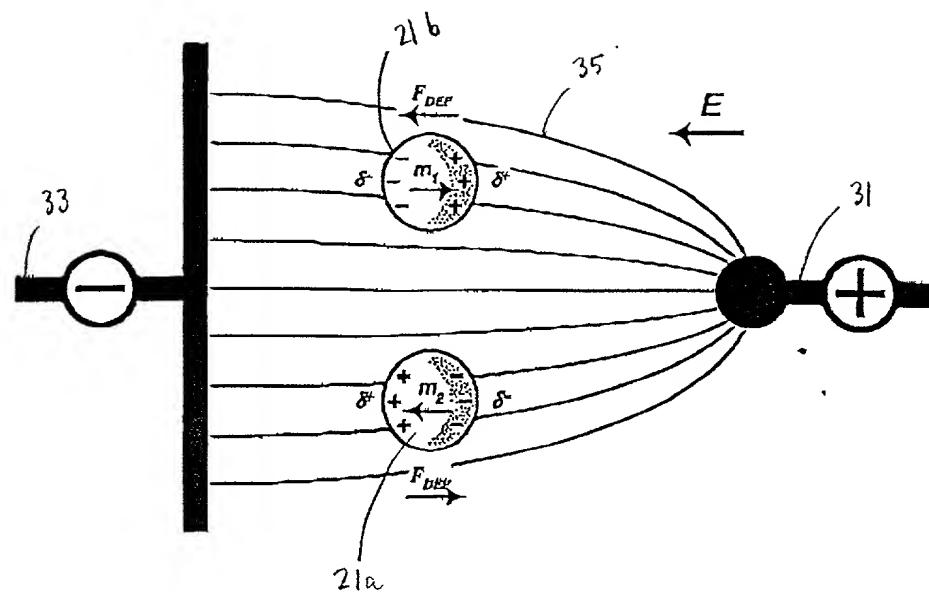


FIG. 2

FIGURE 16.20 16.21 16.22 16.23 16.24

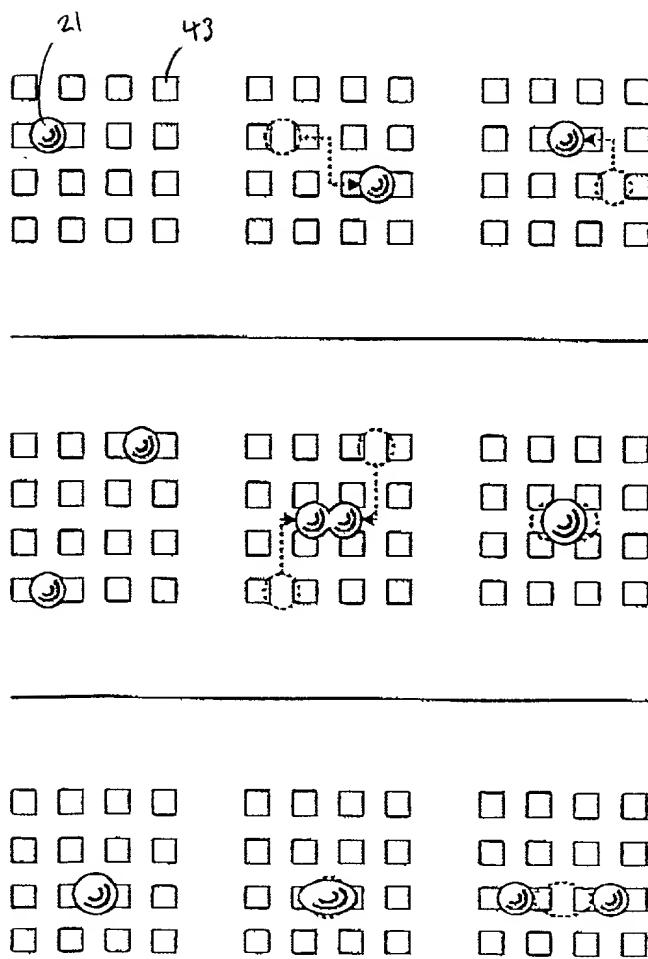


FIG. 12

0 9 6 0 2 6 3 3 0 4 0 0

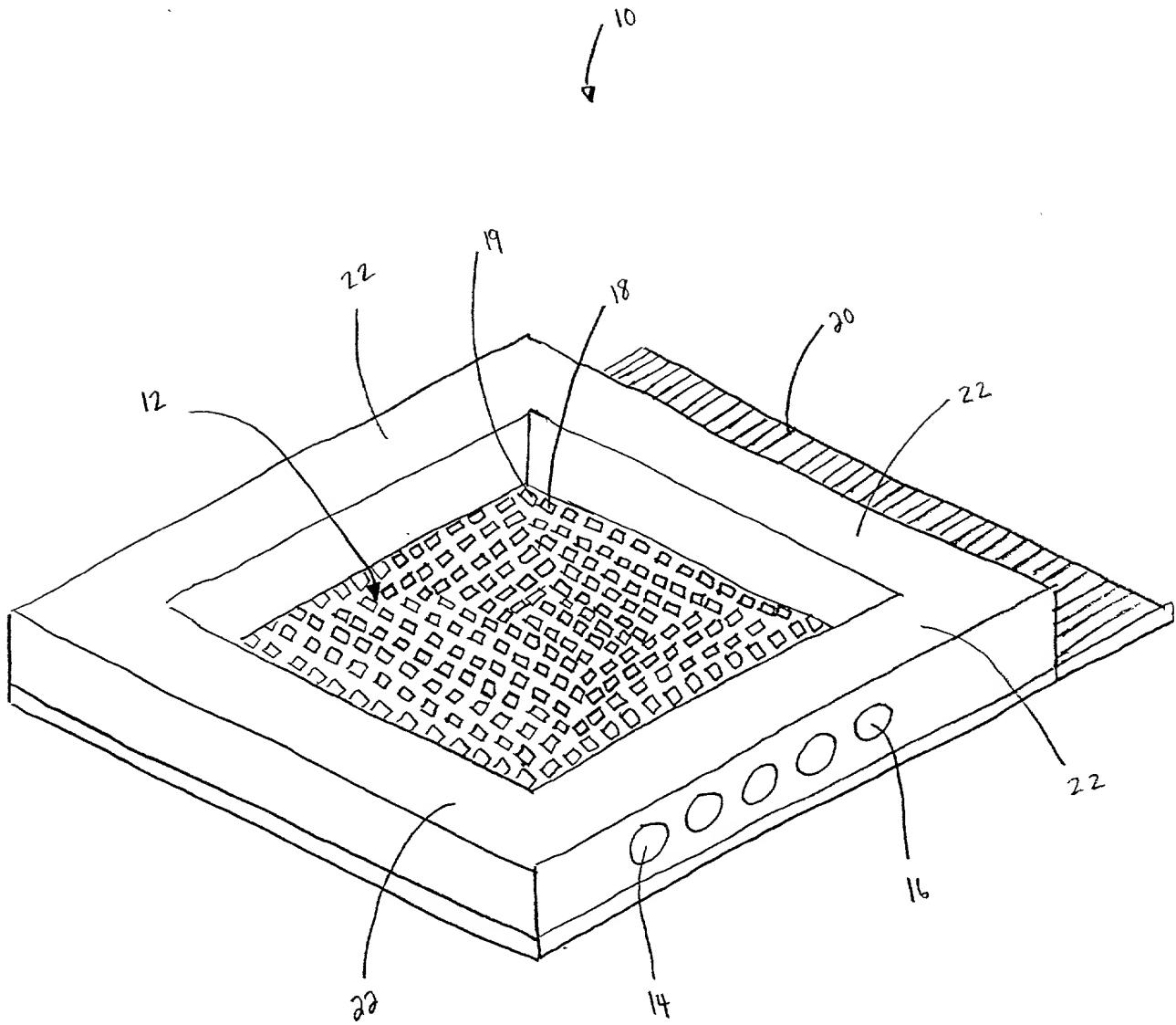


FIG. 4

100000000000000000000000

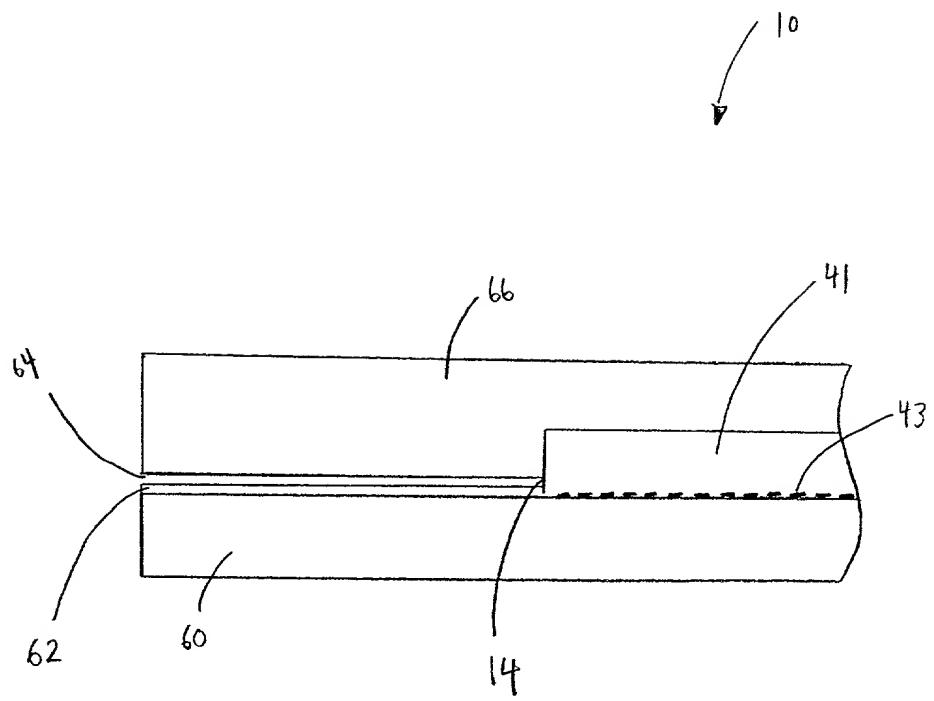


FIG. 5

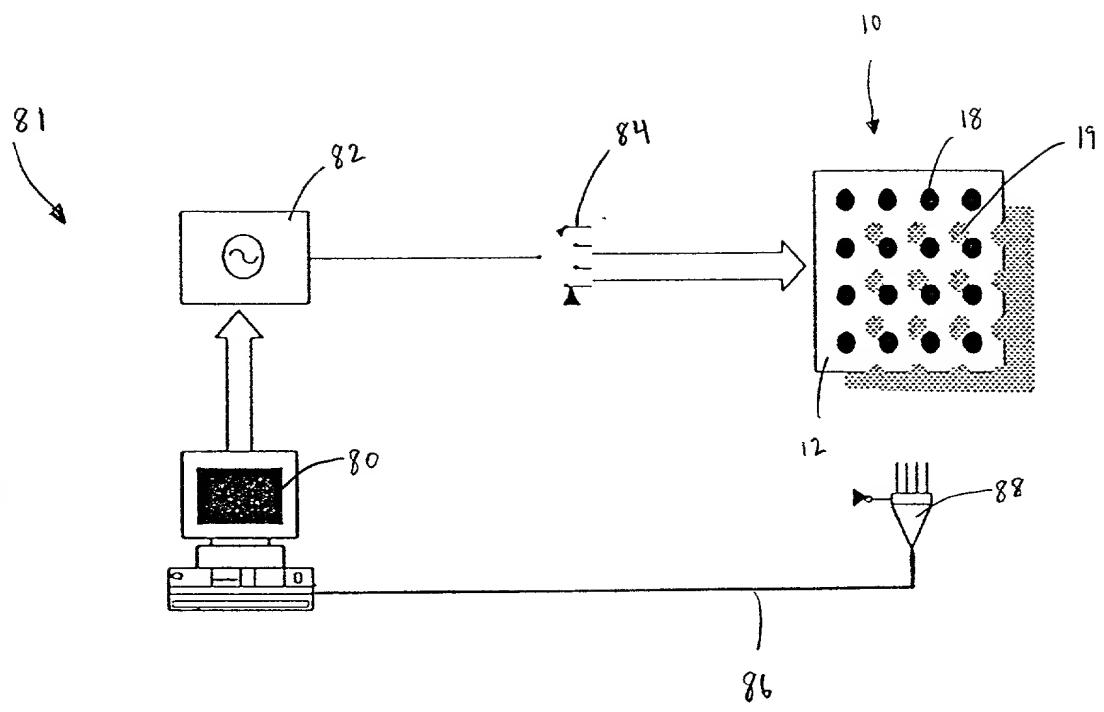


FIG. 6

2005600

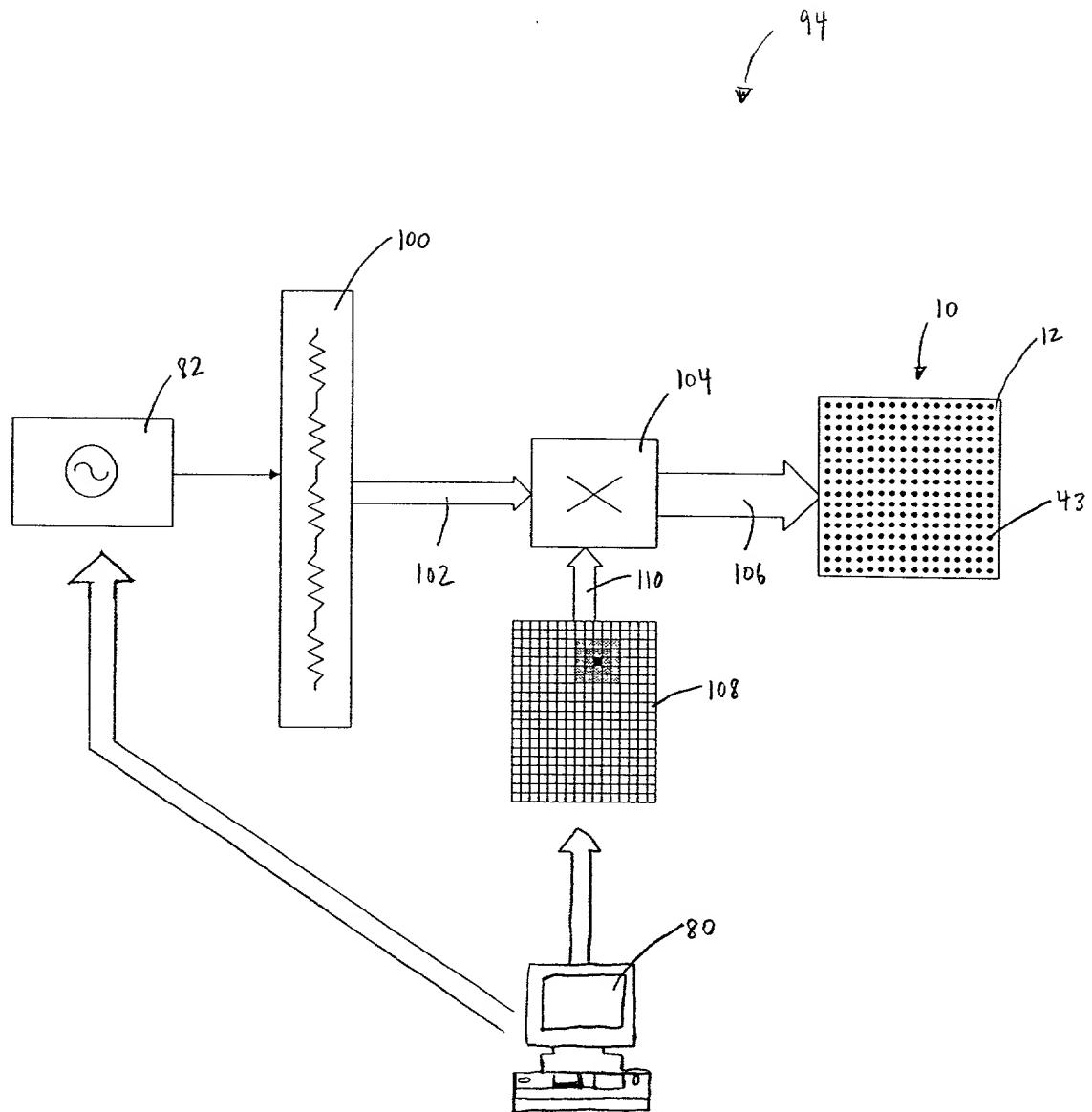
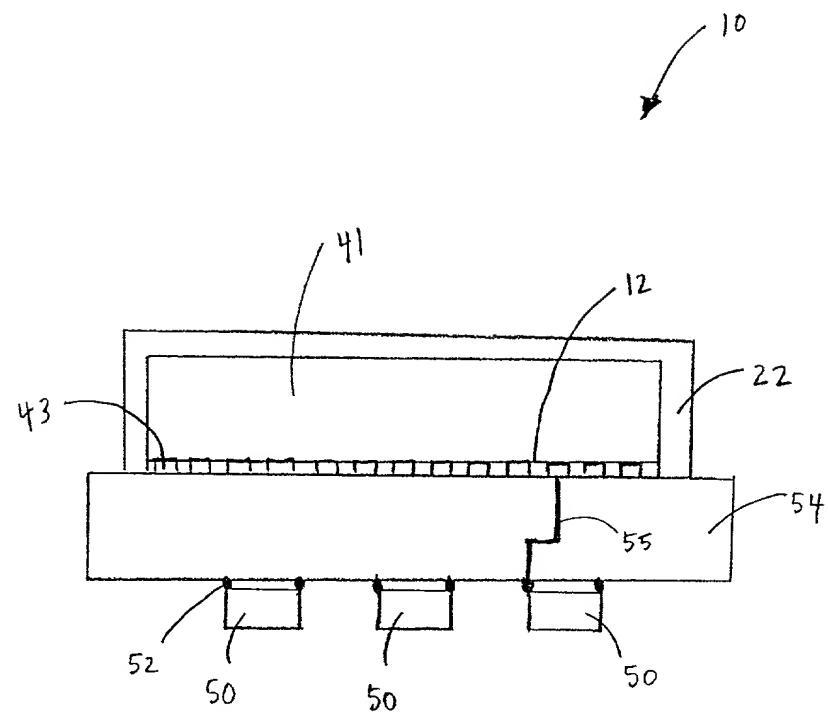


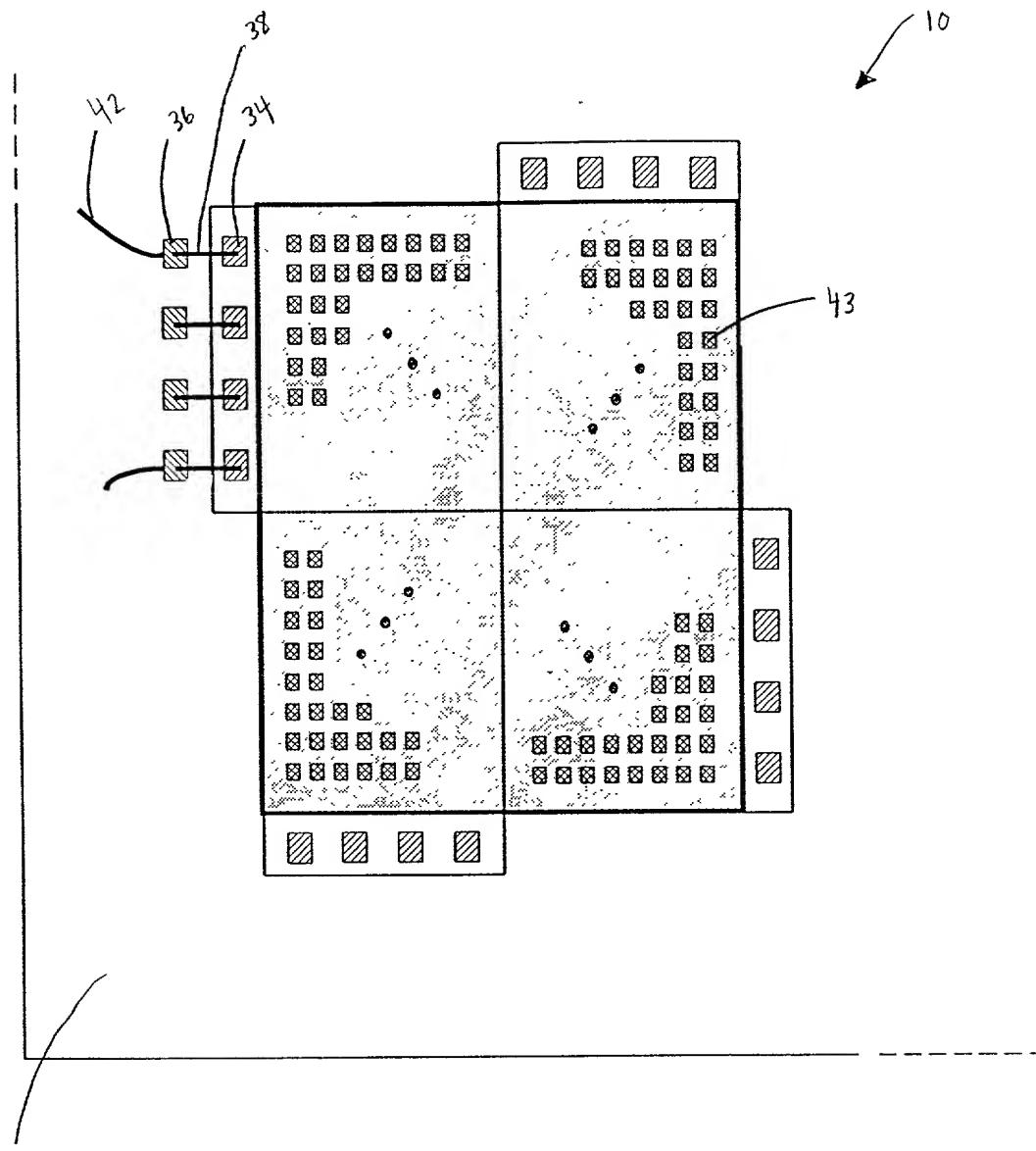
FIG. 7

U.S. Pat. No. 4,320,650



F16. 8

4,001,200 Feb 22, 1976



30

Fig. 9

Multiple programmable inlet/outlet  
ports along edges of processor

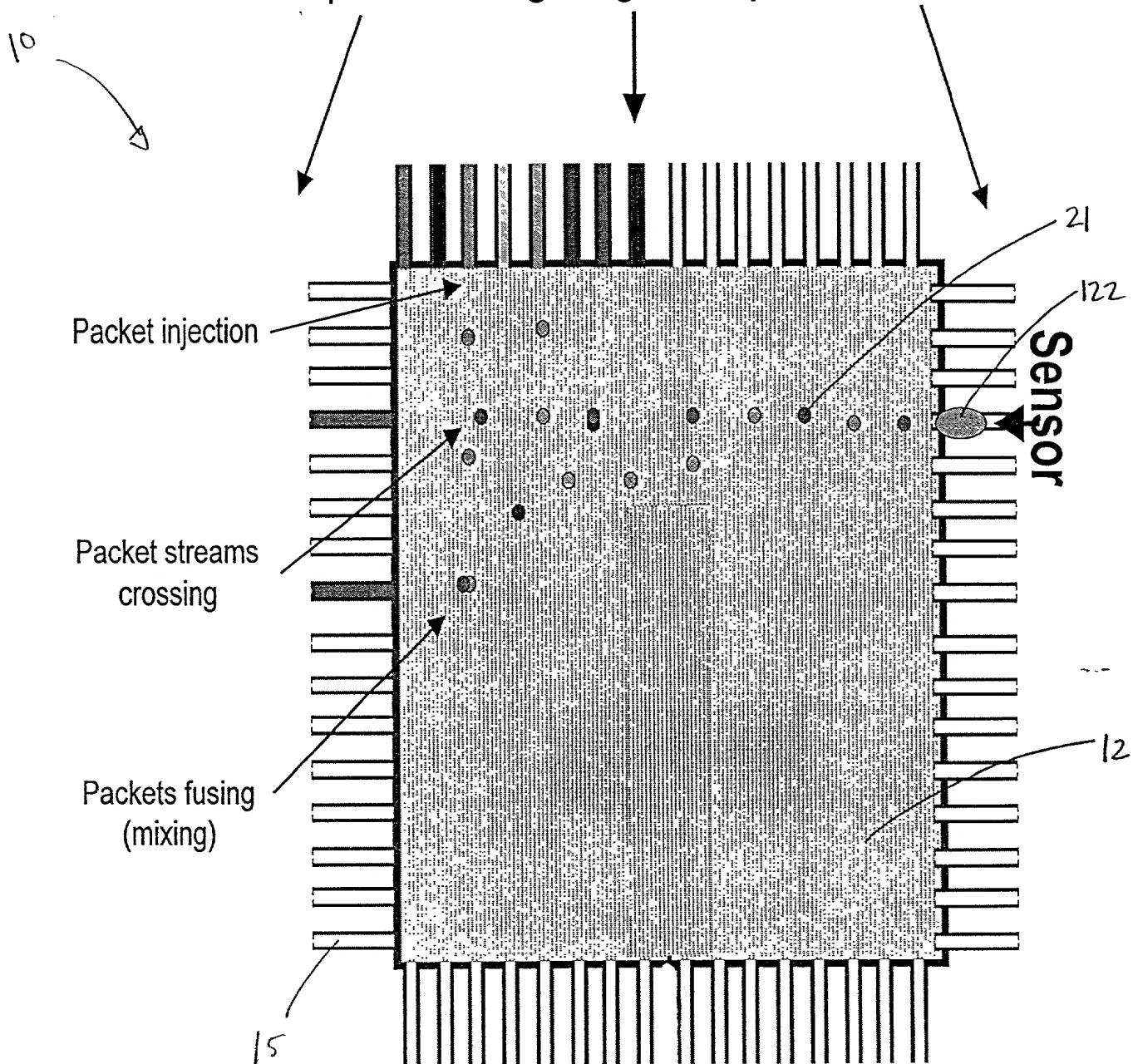


FIG. 9B

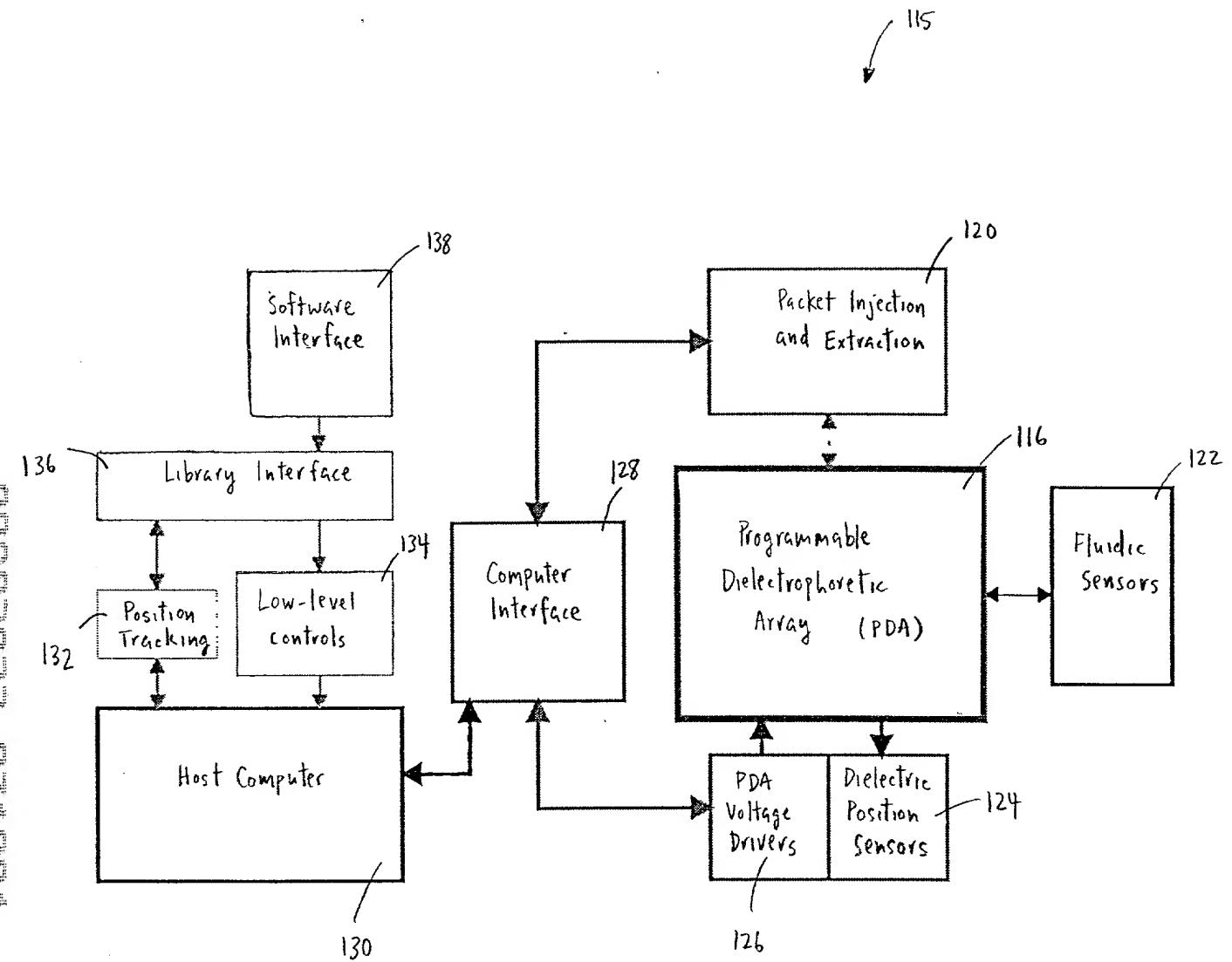


FIG. 10

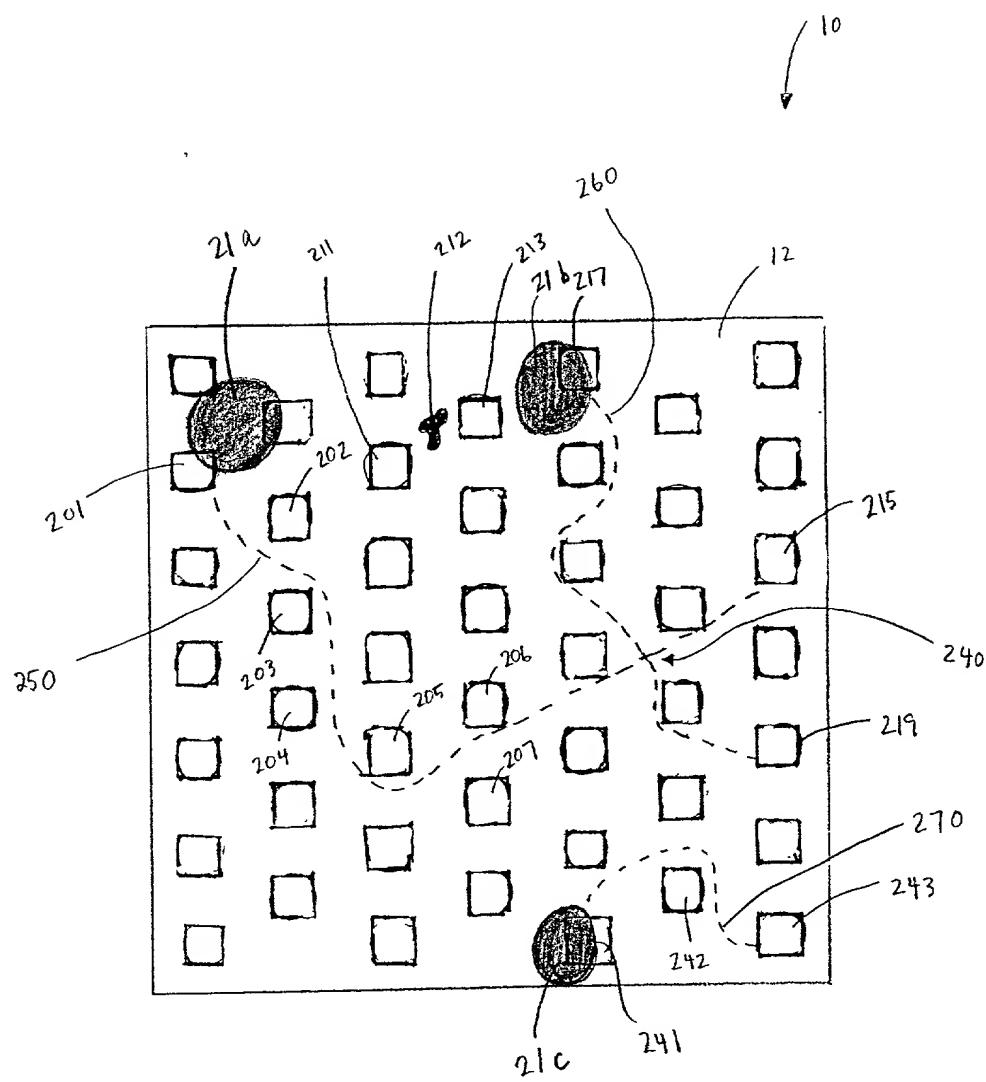


FIG. 11

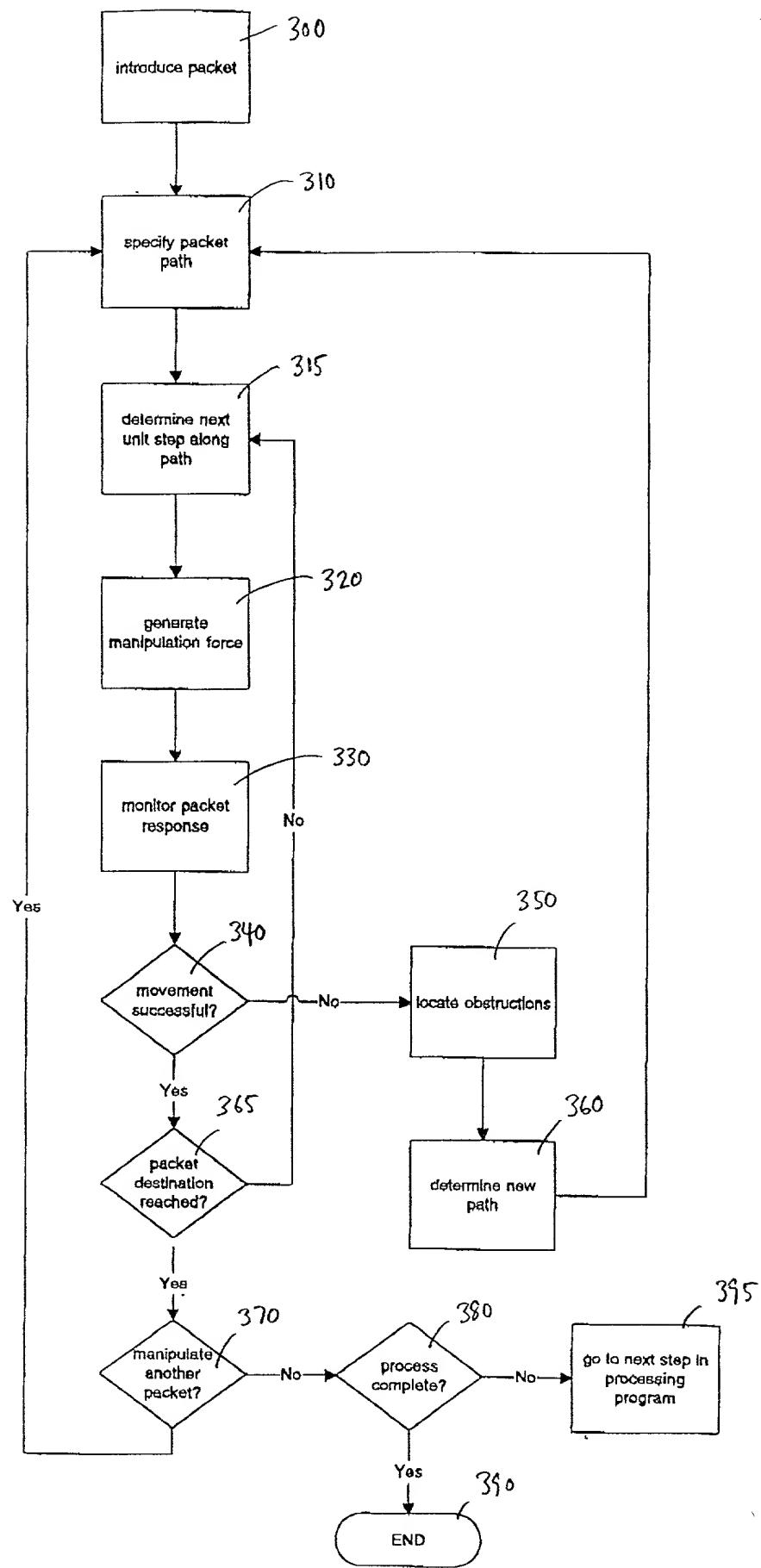


FIG. 13